SPECIFICATION AMENDMENTS

Amend the paragraph that begins in line 2 on page 10 as follows (this paragraph has been amended previously):

The foregoing description has been given on the assumption that the transient current I_G flowing into the logic gate is mostly the short circuit current I_S. With the recent microfabrication of CMOS circuits, wiring delay becomes dominant over the gate delay. This implies that, assuming that the transition time of the input voltage is fixed, the ratio of the charging current I_C to the output signal line OUT is higher than the ratio of the short circuit current I_S in the transient current I_G that flows into the CMOS logic gate. Hence, the time when the waveform of the transient current I_G of the logic gate reaches its peak is dependent on the ~~ration~~ ratio between the capacitance charging current I_C and the short circuit current I_S. When the capacitance charging current I_C is smaller than the short circuit current I_S, the peak of the waveform of the transient current I_G coincides with the peak of the short circuit current I_S. Since the peak of the short circuit current I_S coincides with the time of transition of the input voltage, the peak of the transient current I_G precedes the transition time of the logic gate output. Conversely, when the capacitance charging current I_C is larger than the short circuit current I_S, the peak of the waveform of the transient current I_G concurs with the peak of the current I_C. Since the capacitance charging current I_C is related to the voltage transition on the output signal line OUT, the peak of the transient current I_G virtually coincides with the transition time of the output from the logic gate.

BEST AVAILABLE COPY

PAGE 2/6 * RCVD AT 8/3/2004 2:25:07 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:415 989 0910 * DURATION (mm-ss):02-06